Senior ASIC Verification Engineer

The ideal candidate will have a Bachelor's Degree in Electrical Engineering, Computer Engineering, or Computer Science with five to ten years of experience in the verification of ASIC/FPGA devices.

The following skills and experience are required:

- Strong understanding of verification process and flow
    - Join a project at any phase with minimal disruption
    - Participate as a lead and/or contributor
    - Quickly adapt to a variety of different environments, methods and standards
- Ability to create a high-level verification plan
    - Derivation of verification requirements from design requirements
    - Derivation of project schedule from verification requirements
    - Architecting a complex test environment
    - Identification and integration of re-use
- Ability to create a complex constrained random test environment
    - Setup, build and run test benches
    - Develop agents for complex interfaces (protocol/retries/split transactions)
    - Application of direct and random methods
    - Application of coverage analysis (types and convergence methods)
    - Analyzing and debugging failures to establish root cause
    - Application of assertions
- Strong understanding of Object Oriented Programming (classes, methods, polymorphism)
- Use of a high-level language for verification, such as SystemVerilog C++, Java, etc.
- Experience with verification methodologies (OVM/UVM)
- Highly skilled with one or more industry standard simulation tools such as Mentor Questa-ModelSim, Synopsys VCS, or Cadence NCSIM
- Strong understanding of typical design structures (FIFO's, pipelines, memories, state machines, etc.)
- Strong understanding of standard protocols (PCI Express, Ethernet, etc.)
- Comfortable and confident interacting with customers
- Excellent written and verbal communication skills

The following additional skills and experiences would be a plus:

- Experience verifying hierarchically partitioned large ASICs
- SystemVerilog/C++ co-simulation
- Overall knowledge of the ASIC development process
- RTL design experience
- Ability to train/mentor junior engineers

Must be a US Person as defined in EAR 15 CFR Part 772 and ITAR 22 CFR Section 120.15, which includes US Citizenship, US Permanent Residence, or a Protected Person under 8 U.S.C. 1324b(a)(3).

For consideration, please send your resume to careers@firstpasseng.com