Senior ASIC Back-end Design Engineer

The ideal candidate will have a Bachelor's Degree in Electrical Engineering with five to ten years of experience in synthesis and back-end design of ASIC/IC devices.

Job Description: The candidate will be part of a team responsible for developing, executing and maintaining ASIC/foundry hand-off design flows, and will assume responsibility for supporting all physical aspects thru design tape-out (IO planning, timing, CTS, test insertion, power, noise, area, placement, rule, etc). The candidate will integrate with a variety of disciplines and teams including front-end design, verification, DFX, place and route, and foundry interface. Entry points include design partitioning and floorplanning, developing and executing synthesis strategies, integrating PDKs into development flows, planning design to physical hand-off flows, managing top-level constraints, and integrating foundry quality requirements.

The following skills and experience are required:

- ASIC/IC development flows (component and SoC) for **22nm** and smaller technologies
- Developing floorplanning, partitioning, and synthesis strategies
- Experience with one or more industry standard CAE tool flows (preferably Cadence)
- IP, hard and soft macro integration
- Integration of DFX such as MBIST, scan chain management, scan compression, special test structures, IO planning and boundary scan, clock planning and CTS for test
- Clocking and global signal structures and methods, CTS planning, constraints
- Setup and execution of STA, constraint management and strategies, jitter OCV and noise budgets, reconciling slack violations and closing timing
- Setup and execution of Logical Equivalence Checking

The following additional skills and experiences would be a plus:

- 8G or higher SERDES, PLLs
- 14nm @ > 1 GHz
- Strong working knowledge of physical design
    - Highly directed or manual place and route of timing critical circuits
    - CTS planning, execution, and analysis
    - Power analysis and management, IR drop mapping, power islands, metal migration, PG synthesis.
    - Parasitic extraction
    - DRC/ERC/LVS, analysis and closure
    - Spare cell insertion
- Experience with IBM/Global Foundry technologies
- Experience with critical path Leakage Power Optimization flow
- Memory compilers, MBIST insertion
- UPF flows and power simulation

Must be a US Person as defined in EAR 15 CFR Part 772 and ITAR 22 CFR Section 120.15, which includes US Citizenship, US Permanent Residence, or a Protected Person under 8 U.S.C. 1324b(a)(3).

For consideration, please send your resume to careers@firstpasseng.com