SoC Logic Design and Verification Engineer

Job Description

Oversees definition, design, verification, and documentation for SoC (System on a Chip) development. Determines architecture design, logic design, and system simulation. Defines module interfaces/formats for simulation. Performs Logic design for integration of cell libraries, functional units and sub-systems into SoC full chip designs, Register Transfer Level coding, and simulation for SoCs. Contributes to the development of multidimensional designs involving the layout of complex integrated circuits. Performs all aspects of the SoC design flow from high-level design to synthesis, place and route, timing and power to create a design database that is ready for manufacturing. Analyzes equipment to establish operation infrastructure, conducts experimental tests, and evaluates results. May also review vendor capability to support development.

Key Qualifications

- Deep-submicron SoC technologies and flows
- Previous development of a large SOC
- Capture and documentation of design requirements
- Design partitioning and micro-architecture
- RTL coding (Verilog or VHDL)
- Setup and execution of synthesis and timing closure flows
- Experience with aspects of DFT, JTAG and boundary scan
- Mixed signal design experience and the tools associated with it
- Experience with ASIC P&R tools such as ICC or Silicon Encounter
- Solid understanding of standard design methods
- Synchronous design practices
- Clocking (domain crossing and skew management)
- Solid understanding of I/O planning and buffer selection
- Solid working experience with industry standard CAD tools and ASIC development flows
- Defining, implementing, and deploying verification capabilities, methodologies, and process improvements.
- Use of a high-level language for verification, such as SystemVerilog C++, Java, etc.
- Development and execution of test-plans, test-bench components BFMs, checkers, trackers, scoreboards and functional coverage.
- Experience with SystemVerilog OVM/UVM
- Experience with Object Oriented Programming (classes, methods, polymorphism)
- Hands-on experience with System Verilog coding.
- Highly skilled with one or more industry standard simulation tools such as Mentor's QuestaModelSim, Synopsys's VCS, or Cadence's NCSIM
- Ability to work closely with other analog, logic and verification engineers, micro-architects, and other team members to ensure quality of test-plans, verification environment, and tests.
- Mixed signal behavior model development and simulation
- Experience in a lab environment debugging ASICs

The ideal candidate should exhibit behavioral traits that indicate:

- Comfortable and confident interacting with customers
- Excellent written and verbal communication skills

- Ability to support occasional travel
- Strong problem solving capability and collaborative mindset.
- As part of a growing, dynamic IP team, the candidate must be successful working with a small team and manage multiple tasks and changing requirements, in an innovative environment.
- Experience as a Project or Team Lead

Education and Experience

- Bachelors degree in EE with 10+ years of work experience or Master's degree in EE with 7+ years' work experience

Must be a US Citizen, Permanent US Resident, or currently authorized to work in the U.S. on a full-time basis without future employment sponsorship.

For consideration, please send your resume to careers@firstpasseng.com