Senior ASIC Verification Engineer

The ideal candidate will have a Bachelor's Degree in Electrical Engineering, Computer Engineering, or Computer Science with five to ten years of experience in the verification of ASIC/IC devices.

The following skills and experience are required:

- Ability to create and execute to a high-level verification plan which includes
    - Setup, building and running simulation test benches
    - Application of coverage analysis (code, functional, assertions, etc.)
    - Derivation of verification requirements from design requirements
    - Analyzing and debugging failures to establish root cause
    - Application of direct and random methods
- Use of a high-level language for verification, such as SystemVerilog C++, Java, etc.
- Highly skilled with one or more industry standard simulation tools such as Mentor's Questa-ModelSim, Synopsys's VCS, or Cadence's NCSIM
- Strong understanding of typical design structures such as FIFO's, pipelines, memories, state machines, etc.
- Strong understanding of standard protocols such as PCI Express, Ethernet, etc.
- Strong understanding of device level requirements, micro-architecture, and detailed design descriptions derived from design specifications
- Comfortable and confident interacting with customers
- Excellent written and verbal communication skills
- Ability to support occasional travel

The following additional skills and experiences would be a plus:

- ASIC design experience
- Experience with SystemVerilog OVM/UVM
- Experience with Object Oriented Programming (classes, methods, polymorphism)
- Experience in a lab environment debugging ASICs

Must be a US Citizen, Permanent US Resident, or currently authorized to work in the U.S. on a full-time basis without future employment sponsorship.

For consideration, please send your resume to careers@firstpasseng.com