Job Description:

Senior SOC Design for Test Engineer responsible for defining, implementing, and deploying advanced design-for-test (DFT) and design-for-debug (DFD) methodologies for highly complex digital and/or mixed-signal SOC's and/or IP. You will work as part of the SOC integration team to document DFT specifications. You will develop DFT/DFD methodologies and infrastructure. You will be responsible for all DFT/DFD implementation and/or verification for multiple SOC's and/or IP design projects. You will be responsible for debugging and delivering ATPG test vectors.

Responsibilities

- Work with architects and physical design team to develop Design for Test (DFT) strategy and architecture design, including SCAN, JTAG, MBIST, Scan Compression, ATPG, Fault Simulation and at-speed testing, and generate ATPG test vectors targeting high fault coverage.
- Integrate DFT analysis and insertion tools in the overall ASIC design flow and complete all Test Design Rule Checks.
- Insert DFT logic, including boundary SCAN, SCAN chains, DFT Compression, Logic BIST, TAP controller, Clock Control block, and other DFT IP blocks. Insert and hook up MBIST logic including test wrappers around memories, MBIST controllers, eFuse logic and connect to core and TAP interfaces.
- Work with the logic design team to develop timing constraints required for DFT implementation and work with physical design team for scan chain reordering. Work directly with external vendors involved in implementing DFT features and test vectors, and verify test logic/operation. Run RTL, gate, and gate with SDF simulations to confirm correct functionality of DFT logic.

Minimum qualifications:

- BS or MS degree in Electrical/Computer Engineering or equivalent.
- 10 years of silicon hardware design and verification experience.
- Solid understanding of hardware design fundamentals and SOC principles is required, as well as expertise in Verilog/VHDL coding, CMOS circuits and digital design especially involving multiple clock domains.
- 6 years of experience inserting, testing, and using DFT logic functions (JTAG, BIST, mBIST, scan, boundary scan, ATPG) on multiple chips that have been through tape-out and product ramp.
- Experience developing DFT specifications and driving DFT architecture for complex chips and experience with industry DFT, MBIST, and ATPG tools such as Synopsys TetraMAX, Mentor FastScan, and Cadence DFT/ATPG tools.
- Direct experience in silicon bring-up, debug, and validation of DFT features on ATE, debugging ATPG patterns, Compressed ATPG patterns, MBIST and JTAG related issues.
- Experience with scripting (CSH, Perl, TCL, or Python) and Makefiles is required.
- Due to the nature of work and customer requirements, all candidates must be US Citizens.

Preferred qualifications:

- Substantial experience in architecture and hardware design.

- Hands on experience and a solid understanding of ASIC design, synthesis, simulation and verification flow. Candidate should be capable of writing the RTL code in VHDL, Verilog or System Verilog for a design block, verify using simulation tools & synthesize to gate level netlist.
- Experience in IP integration (memories, Test controllers, TAP, MBIST), simulation and verification tools, such as VCS, NC-Verilog, and waveform debugging tools, and experience with STA constraints development and analysis for DFT modes and SDF simulations.
- Knowledge and experience of timing closure and industry tools like. - Experience with other industry tools such as Spyglass, Jasper, DFT Max, Modus, Tessent, and TestKompress, formal verification tools such Verplex, Formality, etc..
- Experience using EDA Test tools like Design Compiler (RTL to gate level synthesis),
- IEEE 1149.1 and 1149.6 JTAG & Boundary Scan
- Deep knowledge in fault modeling Stuck-at, Transition, Path Delay, Gate-Exhaustive, IDDQ, and other advanced DFT models.
- A history of successfully delivering good hardware design.
- A strong ability to devise, document, and implement processes and methods in a well-organized, robust, and well-communicated manner.